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A Moore's law for Packaging

Abstract:
While Silicon has scaled aggressively by over a factor of a few thousand over the last six decades the progress in packaging has been more modest – a linear factor 4-5 in most cases. In this talk, we will examine the reasons for this lag and what we are doing to fix this imbalance. Packaging is undergoing a renaissance where chip-to-chip interconnects can approach the densities of on-chip interconnects. We will discuss the technologies that are making this happen and how these can change our thinking on architecture and future manufacturing. Specifically, we will discuss two embodiments: Silicon as the next generation packaging substrate, and Flexible electronics using fan-out wafer level processing. Finally, we'll discuss how these developments can help put some intelligence into Artificial Intelligence and bring about change in Medical Engineering.

Biography

Subramanian S. Iyer (Subu) is Distinguished Professor and holds the Charles P. Reames Endowed Chair in the Electrical Engineering Department and a joint appointment in the Materials Science and Engineering Department at the University of California at Los Angeles. He is Director of the Center for Heterogeneous Integration and Performance Scaling (CHIPS). Prior to that he was an IBM Fellow. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, electrical Fuses, embedded DRAM and 45nm technology node used to make the first generation of truly low power portable devices. He also was among the first to commercialize bonded SOI for CMOS applications through a start-up called SiBond LLC. He has published over 300 papers and holds over 70 patents. He was a Master Inventor at IBM. His current technical interests and work lie in the area of advanced packaging constructs for system-level scaling and new integration and computing paradigms as well as the long-term semiconductor and packaging roadmap for logic, memory and other devices. He has received several outstanding technical achievements and corporate awards at IBM. He is an IEEE Fellow, an APS Fellow and a Distinguished Lecturer of the IEEE EDS and EPS as well as it treasurer of EDS and a member of the Board of Governors of IEEE EPS. He is also a Fellow of the National Academy of Inventors. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012.
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